ABSTRACT OF THE DISCLOSURE

Main memory units are each composed of an even number of sub memory units having different addresses. The sub memory units have memory cells, bit lines corresponding to different data terminals with numbers, sense amplifiers, and column switch circuits for connecting the bit lines to data bus lines. Column switch areas of the main memory units are formed in mirror symmetry. Consequently, the sequence of the data terminal numbers of the bit lines in the case of relief where a redundancy memory unit is used can be easily made the same as in the case of non-relief where the redundancy memory unit is not used. As a result, at the time of defect analysis, the sequence of the bit lines need not be taken into account regardless of whether the product is a relief product or non-relief product. This allows a reduction in the time necessary for defect analysis.